ABSTRACT OF THE DISCLOSURE

A method is provided for forming damascene gates and local interconnects a single process. By combining the formation of a damascene gate and local interconnect into a single process, a low cost solution is provided, having the advantages of low resistance wordlines and reduced gate length while reducing or eliminating the local interconnect to gate contact resistance. Further, the present invention provides flexible layout of active area to form small memory cells based upon the damascene gate and local interconnect structure. As such, the present invention is particularly suited for the fabrication of SRAM memory devices.